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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/871,810	06/04/2001	Shunji Nakata	010704	1974

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/871,810	NAKATA ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's arguments filed 11/17/03 have been fully considered but they are not persuasive. The rejection is repeated below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda et al. (U.S. Patent No. 5,994,935) in view of Nakata et al. ("A Low Power Multiplier Using Adiabatic Charging Binary Decision Diagram Circuit", Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pages 444-445.

In reference to claim 1, Ueda discloses in Figure 1, a register circuit (which is seen to be the same as the flip-flop circuit) having a plurality of n-channel MOSFET transistors (MN1-MN10) and a plurality of p-channel MOSFET transistors (MP1-MP4), accepting an input data (DI, DIB), and a clock signal (CK, CKB), and providing an output data (DO, DOB), the clock signal (CK, CKB) being a power clock signal (which is seen to be any clock signal capable of providing power to the circuit) having a rising and falling waveform (the term gradually is not given any patentable weight because it is indefinite). Ueda does not disclose that a charge recycle power source is used to generate the clock signal. Nakata discloses that it is well-known that a switched

capacitor regenerator (see Figure 4) can be used to generate the power clock signal in which power supplied to a load is partially collected and returned to the charge recycle power source, and the inequality ($|V_{TN}| + |V_{TP}| \geqq VDD$) is satisfied. It would have been obvious to one of skill in the art at the time of the invention that the well known switched capacitor regenerator of Nakata could be used in association with the register circuit of Ueda as a means of generating the required clock signals. Since Ueda does not disclose a particular means for generating the clock signals (CK, CKB) any waveform generator could be used and the switched capacitor regenerator is one example of such.

In reference to claim 2, Ueda discloses in the ABSTRACT that the register circuit (flip-flop circuit) comprises two latch circuits (which are seen to be D-latch circuits) with an input of a second D-latch circuit coupled with an output of a first D-latch circuit (which is seen to be the cascade connection of the two latches), a first D-latch circuit accepts a first power clock signal (CK), and a second D-latch circuit accepts a second power clock signal (CKB) which is different by 180° phase of the first power clock signal (which can be seen in Figure 2B).

In reference to claim 3, applicant also discloses in the admitted prior art (see Figure 17) a D-latch circuit (70) comprising a pair of NOR circuits (71, 72) with one of the inputs of each NOR circuit (71, 72) being coupled with an output of the other NOR circuit (71, 72), and a pair of AND circuits (73, 74) each accepting an input data (D, DN) in differential form and a power clock signal (CK), and providing an output to the other

input of each of the NOR circuits (71, 72). This is seen to be an alternate method of designing a D-latch circuit that is well known to one of ordinary skill in the art.

In reference to claim 5, Ueda discloses in Figure 12, a well-known latch circuit comprising a memory element having a first inverter (INV1) providing an output (DO) of the D-latch circuit, a second inverter (INV2) with an input coupled (through transmission gate TG3) with an output of the first inverter (INV1), and a first transmission gate (TG4) connecting an output of the second inverter (INV2) to an input of the first inverter (INV1), and a second transmission gate (TG2) inserted between an input terminal (DIB) and an input of the first inverter (INV1).

Response to Arguments

In response to Applicant's argument that the prior art does not teach the satisfaction of the inequality ($|V_{TN}| + |V_{TP}| \geqq VDD$) and that conventional design of transistor logic does not satisfy the inequality, these arguments are not persuasive. The examiner sees the satisfaction of this inequality as being inherent because the combination of the prior art creates the same structure as claimed. Furthermore, the values used for VDD and the transistor thresholds are seen as design expedients dependent on the particular environment and the desired outcome. In addition, the examiner would like to cite reference 6,046,648 which teaches using values for VDD (Vreg) and the transistor thresholds that would satisfy the inequality for the benefit of reducing power consumption as cited in the reference in column 6, lines 1-13. Therefore, applicant's arguments are not persuasive.

Allowable Subject Matter

4. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: Claim 4 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 11 wherein the register circuit includes a combination logic circuit (40B-D) between the pairs of D-latch circuits (10A-D) in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM and on alternate Fridays from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC

February 9, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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